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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/785,528	02/24/2004	Won Sun Shin	GK001102	1571

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EXAMINER	
LUU, CHUONG A	

ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 08/24/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/785,528	SHIN ET AL.	
	Examiner	Art Unit	
	Chuong A. Luu	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *03* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *6/5/2006*.

2a)☒ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *25-33* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *25-33* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

Applicant's arguments with respect to claims 25-33 have been considered but are moot in view of the new ground(s) of rejection.

PRIOR ART REJECTIONS

Statutory Basis

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

The Rejections

Claims 25-30 are rejected under 35 U.S.C. 102(b) as being anticipated by Miles et al. (U.S. 5,696,666).

Miles discloses an integrated circuit package with

(25) a substrate (14) having a first surface, an opposite second surface, and central throughhole between the first and second surfaces;

a plurality of electrically conductive circuit patterns (18) on each of the first and second surfaces of the substrate (14), wherein the circuit patterns (18) of each of the first and second surfaces of the substrate (14) include a plurality of lands, the circuit patterns of the first surface also include a plurality of bond fingers (26), and at least

some of the circuit patterns of the first surface are electrically connected through the substrate (14) to some of the circuit patterns of the second surface;

a semiconductor chip (12) in said throughole and electrically connected to the bond fingers (26), wherein the semiconductor chip (12) has a first surface with bond pads thereon, and an opposite second surface, the first surface of the semiconductor chip (12) faces in a same direction the first surface of the substrate, and the second surface of the semiconductor chip (12) is flush with the second surface of the substrate (14), wherein the second surface of the semiconductor chip (12) is exposed (see Figure 1);

a hardened encapsulant (16) within said through hole and covering the semiconductor chip (12) and the bond fingers (26), wherein the lands of each of the first and second surfaces are outward of a perimeter of the encapsulant (16) (see Figure 1);

(26) wherein the substrate further comprises a cover coat over the circuit patterns of the first and second surfaces of the substrate, wherein the respective lands and bond fingers are exposed through respective apertures in the cover coat (see Figure 1);

(27) further comprising a plurality of electrically conductive balls, wherein each of the conductive balls is fused to a respective one of the lands of the first surface of the substrate (see Figure 1);

(28) further comprising a plurality of second electrically conductive balls, wherein each of the second electrically conductive balls is fused to a respective one of the lands of the second surface of the substrate (see Figure 1);

(29) further comprising a plurality of electrically conductive balls, wherein some of said electrically conductive balls are fused to respective ones of the lands of the first surface of the substrate and some of said electrically conductive balls are fused to respective ones of the lands of the second surface of the substrate (see Figure 1);

(30) further comprising a plurality of electrically conductive balls, wherein each said electrically conductive ball is fused to a respective one of the lands of the second surface of the substrate (see Figure 1).

PRIOR ART REJECTIONS

Statutory Basis

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The Rejections

Claims 31-33 are rejected under 35 U.S.C. 103(a) as being unpatentable Miles et al. (U.S. 5,696,666) in view of Akram et al. (U.S. 6,313,522 B1).

Miles teaches the above outlined features except for a stackable semiconductor package. However, Akram discloses a stack of semiconductor packages with **(31)** a first semiconductor package comprising: (a) a substrate (18) having a first surface, an

opposite second surface, and central through hole between the first and second surfaces; (b) a plurality of electrically conductive circuit patterns (40, 46, 45) on each of the first and second surfaces of the substrate (18), wherein the circuit patterns (40, 46, 45) of each of the first and second surfaces of the substrate (18) include a plurality of lands, the circuit patterns (40, 46, 45) of the first surface also include a plurality of bond fingers, and at least some of the circuit patterns (40, 46, 45) of the first surface are electrically connected through the substrate (18) to some of the circuit patterns (40, 46, 45) of the second surface that include respective ones of the lands; (c) a semiconductor chip (24B) in said through hole and electrically connected to the bond fingers (27), wherein the semiconductor chip (24B) has a first surface with bond pads thereon, and an opposite second surface, the first surface of the semiconductor chip faces in a same direction as the first surface of the substrate, and the second surface of the semiconductor chip is flush with the second surface of the substrate; (d) a hardened encapsulant within said through hole and covering the semiconductor chip and the bond fingers, wherein the lands of each of the first and second surfaces are outward of a perimeter of the encapsulant; and (e) a plurality of electrically conductive balls, wherein each of the conductive balls is fused to a respective one of the lands of the first surface of the substrate; a second semiconductor package comprising a plurality of second electrically conductive balls, wherein the second semiconductor package is in a stack with the first semiconductor package, and the second electrically conductive balls of the second package each superimpose and are electrically connected to a respective one of the lands of the second surface of the substrate of the first semiconductor package

(see Figures 2-3); **(32)** wherein the second semiconductor package includes a second substrate with a central second through hole, the second semiconductor chip is in the second through hole, and the second semiconductor package further comprises a hardened second encapsulant in the second through hole and covering the second semiconductor chip (see Figures 2-3); **(33)** wherein the substrate of the first package further comprises a cover coat over the circuit patterns of the first and second surfaces of the substrate, wherein the respective lands and bond fingers are exposed through respective apertures in the cover coat (see Figures 2-3). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the Miles's device (accordance with the teaching of Akram). Doing so would facilitate the manufacture of the semiconductor device and increase the speed of the semiconductor structure.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the

shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chuong A. Luu whose telephone number is (571) 272-1902. The examiner can normally be reached on M-F (6:15-2:45).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Smith can be reached on (571) 272-1907. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Chuong Anh Luu
Patent Examiner
August 07, 2006